

**Chapter 1 : Differential, Multistage and Operational Amplifiers 1-1 to 1-41**

**Syllabus :** Differential amplifier; Power amplifier; Direct coupled multi-stage amplifier; Internal structure of an operational amplifier, Ideal op-amp, Non idealities in op-amp (Output offset voltage, Input bias current, Input offset current, Slew rate, Gain bandwidth product).

1.1 Introduction ..... 1-2

1.2 Ideal Differential Amplifier ..... 1-2

    1.2.1 Differential Gain  $A_d$  ..... 1-2

    1.2.2 Common Mode Gain  $A_c$  ..... 1-2

    1.2.3 Common Mode Rejection Ratio (CMRR) ..... 1-3

1.3 Basic BJT Differential Amplifier ..... 1-3

    1.3.1 Differential Amplifier Configurations ..... 1-5

    1.3.2 Features of a Differential Amplifier ..... 1-6

    1.3.3 Advantages of DIFF-AMP ..... 1-6

1.4 Multistage Amplifiers ..... 1-6

    1.4.1 Cascaded Amplifier ..... 1-6

    1.4.2 Gain of the Cascaded Configuration ..... 1-6

    1.4.3 n-stage Cascaded Amplifier ..... 1-7

    1.4.4 DC Amplifier ..... 1-7

    1.4.5 R-C Coupled Amplifiers ..... 1-7

    1.4.6 Direct Coupled Amplifiers ..... 1-8

1.5 Power Amplifier ..... 1-9

    1.5.1 Important Features of a Power Amplifier ..... 1-9

    1.5.2 Conversion Efficiency ..... 1-10

    1.5.3 Classification of Power Amplifiers ..... 1-10

    1.5.4 Class A Power Amplifier ..... 1-10

    1.5.5 Class B Amplifier ..... 1-11

    1.5.6 Class AB Amplifier ..... 1-12

    1.5.7 Class C Amplifiers ..... 1-13

1.5.8 Comparison of Power Amplifiers ..... 1-13

1.6 Class B Power Amplifiers ..... 1-14

    1.6.1 Class B - Push Pull Amplifier ..... 1-14

    1.6.2 Cross-over Distortion in Class B Amplifiers ..... 1-15

    1.6.3 Advantages of Class B Amplifier ..... 1-16

    1.6.4 Disadvantages ..... 1-16

    1.6.5 Complementary Symmetry Class B Amplifier (Without Transformer) ..... 1-16

    1.6.6 Comparison of Class B Push-pull and Complementary Symmetry Circuits ..... 1-17

    1.6.7 Complementary Push Pull and Crossover Distortion ..... 1-18

1.7 Class AB Push Pull Amplifier ..... 1-18

    1.7.1 Complementary Symmetry Class AB Amplifier ..... 1-19

    1.7.2 Complementary Symmetry Class AB Amplifier Using Diodes for Biasing ..... 1-19

1.8 OP-AMP ..... 1-20

    1.8.1 Applications of OP-AMP ..... 1-20

1.9 Why is it Called Operational Amplifier ? ..... 1-20

    1.9.1 Advantages of OP-AMP ..... 1-20

    1.9.2 Need of an OPAMP ..... 1-20

1.10 OP - AMP Symbol and Terminals ..... 1-21

    1.10.1 Symbol and Terminals ..... 1-21

    1.10.2 DC Power Supply for an OP-AMP ..... 1-21

1.11 Equivalent Circuit of an OP-AMP ..... 1-22

1.12 Internal Structure of a OP-AMP ..... 1-22

1.13 OP-AMP Parameters (Characteristics) ..... 1-23

1.14 An Ideal OP-AMP ..... 1-27

    1.14.1 Important Characteristics of the Ideal OP-AMP ..... 1-28



1.15	Voltage Transfer Characteristics of an Ideal OP-AMP .....1-28	2.2	Open Loop and Closed Loop Configurations of OP-AMP .....2-2
1.16	OP-AMP 741 .....1-29	2.2.1	Open Loop Configuration of OP-AMP .....2-2
1.16.1	Pin Configuration .....1-29	2.2.2	OP-AMP in Closed Loop Configurations ..2-2
1.16.2	Comparison of Ideal and Practical OP-AMP .....1-30	2.2.3	Advantages of Negative Feedback .....2-3
1.17	Practical OP-AMP Characteristics (Parameters) .....1-30	2.2.4	Concept of Virtual Short and Virtual Ground .....2-3
1.18	Input Bias and Offset Currents .....1-30	2.3	Idealized Analysis of Op-amp Circuits .....2-4
1.18.1	Input Bias Current .....1-30	2.4	The Inverting Amplifier .....2-4
1.18.2	Input Offset Current ( $I_{ios}$ ) .....1-31	2.4.1	Ideal Closed Loop Characteristics .....2-5
1.18.3	Effect of Bias Currents .....1-31	2.5	Non-Inverting Amplifier .....2-6
1.18.4	Input Bias Current Compensation .....1-31	2.5.1	Ideal Closed - Loop Characteristics .....2-6
1.18.5	Effect of Input Offset Current .....1-32	2.5.2	Solved Examples on Ideal Inverting and Non-Inverting Amplifiers .....2-7
1.19	Input Offset Voltage ( $V_{ios}$ ) .....1-33	2.6	The Voltage Follower .....2-8
1.19.1	Effect of Input Offset Voltage .....1-33	2.6.1	Inverter (Sign Changer) .....2-9
1.19.2	Input Offset Voltage Compensation .....1-34	2.7	Adder .....2-10
1.19.3	Total Input Offset Voltage .....1-34	2.7.1	Inverting Adder or Inverting Summing Amplifier .....2-10
1.19.4	Total Output Offset Voltage ( $V_{oos}$ ) .....1-35	2.7.2	Scaling or Weighted Amplifier .....2-11
1.20	Slew Rate .....1-35	2.7.3	Averaging Circuit .....2-11
1.20.1	Causes of Slew Rate .....1-36	2.8	Differential Amplifier .....2-12
1.21	Solved University Examples (New Syllabus) .....1-40	2.8.1	Difference Amplifier using One OP-AMP .....2-12
1.22	University Questions and Answers (New Syllabus) .....1-40	2.8.2	Subtractor .....2-13
	• <b>Review Questions</b> ..... <b>1-37</b>	2.8.3	Differential Amplifier with Two OP-AMPs .....2-13
	• <b>MCQs with Answers</b> ..... <b>1-38</b>	2.8.4	High Input Impedance Difference Amplifier (With three OP-AMPs) .....2-14
<b>Chapter 2 : Linear Applications of OP-AMP 2-1 to 2-58</b>		2.9	Instrumentation Amplifier .....2-15
<b>Syllabus</b> : Idealized analysis of op-amp circuits, Inverting and non-inverting amplifier, Differential amplifier, Instrumentation amplifier, Integrator, Active filter, P, PI and PID controllers and lead/lag compensator using an op-amp, Voltage regulator, Oscillators (Phase shift, Wien bridge), Analog to Digital conversion.		2.9.1	Requirements of an Instrumentation Amplifier .....2-15
2.1	Linear Applications of OPAMP ..... 2-2		



2.9.2	The Three OP-AMP Instrumentation Amplifier .....	2-16	2.13.1	First Order Butterworth Low-pass Filter .....	2-29
2.9.3	Advantages of Instrumentation Amplifiers .....	2-17	2.13.2	Second Order Low-pass Butterworth Filter .....	2-30
2.9.4	Applications of Instrumentation Amplifier .....	2-17	2.14	Butterworth High-pass Filters .....	2-31
2.10	Integrator .....	2-18	2.14.1	First Order Butterworth High-pass Filter .....	2-31
2.10.1	Ideal Integrator Circuit .....	2-18	2.14.2	Second Order High-pass Butterworth Filter .....	2-33
2.10.2	Input and Output Waveforms .....	2-18	2.15	Band pass Filter .....	2-34
2.10.3	Problems Associated with the Ideal Integrator .....	2-19	2.16	Band-Reject Filter .....	2-35
2.10.4	Practical Integrator .....	2-20	2.17	All Pass Filter .....	2-35
2.10.5	Design Procedure for an Integrator .....	2-20	2.18	Controllers .....	2-36
2.10.6	Applications of an Integrator .....	2-21	2.18.1	Classification of Controllers .....	2-36
2.11	Differentiator .....	2-21	2.18.2	Advantages of Electronic Controllers .....	2-36
2.11.1	Basic or Ideal Differentiator Circuit .....	2-21	2.18.3	Disadvantage .....	2-36
2.11.2	Input and Output Voltage Waveforms .....	2-22	2.19	Analog Electronic Controllers .....	2-36
2.11.3	Practical Differentiator .....	2-22	2.19.1	Proportional (P) Controller .....	2-36
2.11.4	Steps to Design a Practical Differentiator .....	2-23	2.19.2	Integral (I) Controller .....	2-37
2.11.5	Applications of a Differentiator .....	2-23	2.19.3	PI Controller .....	2-37
2.12	Active Filters .....	2-23	2.19.4	(PID) Controller .....	2-38
2.12.1	Merits and Demerits of Active Filters Over Passive Filters .....	2-24	2.19.5	Temperature Control using PID Controller .....	2-39
2.12.2	Comparison of Active and Passive Filters .....	2-25	2.20	Lead-lag Compensator .....	2-39
2.12.3	Filter Types .....	2-25	2.20.1	Frequency Response .....	2-39
2.12.4	Definitions Related to Filters .....	2-25	2.20.2	Open Loop Frequency Response of Internally Compensated OP-AMP .....	2-39
2.12.5	Frequency Response Characteristics of Filters .....	2-26	2.20.3	What is Stability ? .....	2-40
2.12.6	Q of a Filter .....	2-28	2.20.4	Lead-Lag (Pole – Zero) Compensator .....	2-41
2.12.7	Butterworth Response or Alignment .....	2-28	2.21	Introduction to Voltage Regulators .....	2-42
2.13	Butterworth Low-pass Filters .....	2-29	2.21.1	Regulated Power Supply .....	2-42
			2.21.2	Parameters of a Power Supply .....	2-42



<p>2.22 IC Voltage Regulators .....2-44</p> <p>    2.22.1 Classification of IC Voltage Regulators ...2-44</p> <p>2.23 Three Terminal IC Regulators .....2-44</p> <p>    2.23.1 Advantages of IC Regulators .....2-44</p> <p>    2.23.2 Block Diagram of a Three Pin IC Voltage Regulator .....2-44</p> <p>2.24 Three Terminal Fixed Voltage Regulators .....2-45</p> <p>    2.24.1 78XX Series (Fixed Positive Voltage Regulator .....2-45</p> <p>    2.24.2 79XX Series (Fixed Negative Voltage Regulator).....2-45</p> <p>    2.24.3 Standard Connections for Positive Fixed Voltage Regulator (78XX) .....2-46</p> <p>    2.24.4 Negative Fixed Voltage Regulators (79XX Series) .....2-46</p> <p>    2.24.5 Applications of Three Pin Voltage Regulators .....2-47</p> <p>2.25 Three Terminal Adjustable Voltage Regulators .....2-47</p> <p>    2.25.1 Adjustable Positive Voltage Regulator (LM 317) .....2-48</p> <p>    2.25.2 Typical connection diagram for LM 317 regulator .....2-48</p> <p>    2.25.3 Practical Regulator using LM 317 .....2-49</p> <p>    2.25.4 Comparison of 78 XX and LM 317 Regulators .....2-49</p> <p>    2.25.5 Applications of LM 317 .....2-50</p> <p>2.26 Sine Wave Oscillators .....2-50</p> <p>2.27 RC Phase Shift Oscillator .....2-50</p> <p>    2.27.1 RC Network for the Phase Shift Oscillator.....2-50</p> <p>    2.27.2 RC Phase Shift Oscillator using OP-AMP .....2-50</p> <p>2.28 Wien Bridge Oscillator.....2-52</p> <p>    2.28.1 The Wien Bridge Circuit .....2-52</p>	<p>    2.28.2 Wien Bridge Oscillator using OP-AMP .....2-53</p> <p>    2.28.3 Comparison of Wien Bridge and R-C Phase Shift Oscillators .....2-54</p> <p>2.29 University Questions and Answers (New Syllabus) .....2-58</p> <ul style="list-style-type: none"> <li>• <b>Review Questions.....2-55</b></li> <li>• <b>MCQs with Answers .....2-56</b></li> </ul> <hr/> <p><b>Chapter 3 : Nonlinear Applications of OP-AMP</b></p> <p style="text-align: right;"><b>3-1 to 3-28</b></p> <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> <p><b>Syllabus</b> : Hysteretic Comparator, Zero crossing detector, Square-wave and Triangular-wave generators, Precision rectifiers, Peak detector.</p> </div> <p>3.1 Introduction .....3-2</p> <p>    3.1.1 Nonlinear Applications .....3-2</p> <p>3.2 Comparator .....3-2</p> <p>    3.2.1 OP-AMP as a Voltage Comparator .....3-3</p> <p>    3.2.2 Types of Comparator .....3-4</p> <p>3.3 Non-inverting Comparator .....3-4</p> <p>    3.3.1 Transfer Characteristics of Non-inverting Comparator .....3-5</p> <p>3.4 Inverting Comparator .....3-5</p> <p>    3.4.1 Transfer Characteristics of an Inverting Comparator .....3-6</p> <p>3.5 Comparator Characteristics .....3-6</p> <p>    3.5.1 Comparison of Inverting and Non-inverting type Comparators .....3-7</p> <p>    3.5.2 Limitations of OP-AMP as Comparator .....3-7</p> <p>    3.5.3 Requirements of an OP-AMP to be used as a Comparator .....3-7</p> <p>3.6 Zero Crossing Detector .....3-8</p> <p>    3.6.1 Inverting ZCD .....3-8</p> <p>    3.6.2 Non-Inverting ZCD .....3-8</p>
--	---



3.7	Comparator Applications .....	3-9	3.13.1	Positive Peak Detector .....	3-23
	3.7.1 Window Comparators .....	3-9	3.13.2	Negative Peak Detector .....	3-24
3.8	Schmitt Trigger (Hysteretic Comparator) .....	3-10	3.13.3	Peak to Peak Detector .....	3-24
	3.8.1 Types of Schmitt Trigger .....	3-10	3.13.4	Applications .....	3-25
	3.8.2 Inverting Schmitt Trigger .....	3-10	3.14	University Questions and Answers.....	3-28
	3.8.3 Hysteresis .....	3-12	3.15	University Questions and Answers (New Syllabus) .....	3-28
	3.8.4 Comparison of Comparator and Schmitt Trigger .....	3-12		• <b>Review Questions</b> .....	<b>3-25</b>
	3.8.5 Advantages of Schmitt Trigger .....	3-13		• <b>MCQs with Answers</b> .....	<b>3-28</b>
	3.8.6 Solved Examples on Schmitt Trigger .....	3-13	<hr/>		
	3.8.7 Applications of Schmitt Trigger .....	3-14	<b>Chapter 4 : Combinational Digital Circuits 4-1 to 4-44</b>		
3.9	Waveform Generator .....	3-14	<b>Syllabus</b> : Combinational digital circuits, Standard representation for logic functions, K-map representation, Simplification of logic functions using K-map, Minimization of logical functions, Don't care conditions, Q-M method of function realization.		
3.10	Square Wave Generator .....	3-14	4.1	System or Circuit .....	4-2
	3.10.1 Asymmetrical Square Wave Generator ...	3-16		4.1.1 Digital Systems .....	4-2
3.11	Triangular Wave Generator .....	3-16		4.1.2 Types of Digital Circuits .....	4-2
	3.11.1 Triangular Wave Generator using Comparator and Integrator .....	3-17		4.1.3 Combinational Circuit Design .....	4-2
	3.11.2 Modification in the Triangular Wave Generator to Get Sawtooth Output .....	3-18	4.2	SOP and POS Forms .....	4-3
	3.11.3 Sawtooth Generator Using Comparator and Integrator .....	3-18		4.2.1 Sum-of-Products (SOP) Form .....	4-3
3.12	Precision Rectifiers .....	3-19		4.2.2 Product of the Sums Form (POS) .....	4-4
	3.12.1 Precision Half Wave Rectifier .....	3-19		4.2.3 Standard or Canonical SOP and POS Forms .....	4-4
	3.12.2 Non-Inverting Type Precision HWR .....	3-19		4.2.4 Conversion of a Logic Expression to Standard SOP or POS Form .....	4-5
	3.12.3 Inverting Type Precision Half Wave Rectifier .....	3-20		4.2.5 Concepts of Minterm and Maxterm .....	4-6
	3.12.4 Precision Full Wave Rectifiers .....	3-21		4.2.6 Representation of Logical Expressions using Minterms and Maxterms .....	4-7
	3.12.5 Inverting Precision Full Wave Rectifier ...	3-21		4.2.7 Writing SOP and POS Forms for a Given Truth Table .....	4-7
	3.12.6 Advantages of Precision Rectifiers Over Conventional Rectifiers .....	3-23		4.2.8 To Write Standard SOP Expression for a Given Truth Table .....	4-7
	3.12.7 Applications .....	3-23			
3.13	Peak Detector using OP-AMP .....	3-23			



4.2.9	To Write Standard SOP Expression for a Given Truth Table .....	4-8	4.7	Product of Sum (POS) Simplification .....	4-29
4.2.10	Conversion from SOP to POS and Vice Versa .....	4-8	4.7.1	K-map Representation of POS Form .....	4-29
4.3	Methods to Simplify the Boolean Functions .....	4-9	4.7.2	Representation of Standard POS Form on K-map .....	4-29
4.3.1	Algebraic Simplification .....	4-10	4.7.3	Simplification of Standard POS Form using K-map .....	4-30
4.3.2	Disadvantages of Algebraic Method of Simplification .....	4-11	4.8	Quine Mc-Cluskey Minimization Technique (Tabular Method) .....	4-33
4.4	Karnaugh-Map Simplification (The Map Method) .....	4-11	4.8.1	Important Definitions .....	4-34
4.4.1	K-map Structure .....	4-11	4.8.2	Comparison of K-map and Tabular Method .....	4-40
4.4.2	K-map Boxes and Associated Product Terms .....	4-12	4.9	Realizing Logic Functions With Gates .....	4-40
4.4.3	Alternative Way to Label the K-map .....	4-12	4.9.1	Gates .....	4-40
4.4.4	Truth Table to K-map .....	4-13	4.9.2	The EX-OR and EX-NOR Gates in Function Realization .....	4-40
4.4.5	Representation of Standard SOP Form on K-map .....	4-14	4.10	University Questions and Answers .....	4-44
4.5	Simplification of Boolean Expressions using K-map .....	4-14	4.11	University Questions and Answers (New Syllabus) .....	4-44
4.5.1	How does Simplification Take Place ? .....	4-15		• <b>Review Questions</b> .....	<b>4-42</b>
4.5.2	Way of Grouping (Pairs, Quads and Octets) .....	4-15		• <b>MCQs with Answers</b> .....	<b>4-42</b>
4.5.3	Grouping Two Adjacent One's (Pairs) .....	4-15	<hr/>		
4.5.4	Grouping Four Adjacent Ones (Quad) .....	4-16	<b>Chapter 5 : Combinational Logic Circuit Design</b>		
4.5.5	Grouping Eight Adjacent Ones (Octet) .....	4-18	<b>5-1 to 5-58</b>		
4.5.6	Summary of Rules Followed for K-Map Simplification .....	4-18	<b>Syllabus</b> : Multiplexer, De-Multiplexer / Decoders, Adders, Subtractors, BCD arithmetic, Carry look ahead adder, Serial adder, ALU, Elementary ALU design, Popular MSI chips, Digital comparator, Parity checker / generator, Code converters, Priority encoders, Decoders / drivers for display devices.		
4.6	Minimization of SOP Expressions (K-Map Simplification) .....	4-18	5.1	Introduction to Combinational Circuits .....	5-2
4.6.1	Elimination of a Redundant Group .....	4-21	5.1.1	Analysis of a Combinational Circuit .....	5-2
4.6.2	Minimization of Logic Functions not Specified in Standard SOP Form .....	4-21	5.1.2	Combinational Design Examples .....	5-3
4.6.3	Don't Care Conditions .....	4-22	5.2	Combinational Logic with MSI Circuits .....	5-5
4.6.4	Disadvantages of K-Map Technique .....	4-23	5.3	Multiplexer (Data Selector) .....	5-5
			5.3.1	Necessity of Multiplexers .....	5-6



5.3.2	Advantages of Multiplexers .....	5-6	5.10.3	Full Subtractor using Half Subtractors ....	5-23
5.4	Types of Multiplexers .....	5-6	5.11	The n-Bit Parallel Adder .....	5-24
5.4.1	2:1 Multiplexer .....	5-6	5.11.1	A Four Bit Parallel Adder Using Full Adders .....	5-24
5.4.2	A 4:1 Multiplexer .....	5-7	5.11.2	Propagation Delay in Parallel Adder .....	5-24
5.4.3	8:1 Multiplexer .....	5-7	5.11.3	Look Ahead – Carry Adder .....	5-25
5.4.4	16:1 MUX .....	5-8	5.11.4	Four Bit Fast Adder with Look-Ahead Carry .....	5-26
5.4.5	Applications of a Multiplexer .....	5-8	5.11.5	Fast Adder IC 74 LS 83 / 74 LS 283 .....	5-26
5.5	Multiplexer Tree .....	5-8	5.11.6	Four Bit Binary Adder using IC 7483 .....	5-27
5.6	Correspondence between K-map and MUX .....	5-9	5.12	n-bit Parallel Subtractor (Use of Adder as Subtractor) .....	5-27
5.7	Combinational Logic Design with Multiplexers .....	5-9	5.12.1	4 Bit Parallel Subtractor using 2's Complement .....	5-27
5.7.1	Use of 8:1 MUX to Realize a 4 Variable Function .....	5-10	5.12.2	4-Bit Binary Parallel Adder/Subtractor.....	5-28
5.7.2	Implementation of Boolean Expression with Don't Care Conditions .....	5-11	5.13	BCD Arithmetic .....	5-28
5.7.3	Implementing a Standard POS Expression using Multiplexer .....	5-12	5.13.1	BCD Addition .....	5-28
5.8	Demultiplexers .....	5-14	5.13.2	BCD Subtraction .....	5-30
5.8.1	Demultiplexer Principle .....	5-14	5.14	BCD Adder using IC 7483 .....	5-30
5.8.2	Types of Demultiplexers .....	5-14	5.15	Code Converters .....	5-32
5.8.3	Applications of Demultiplexer .....	5-16	5.15.1	Binary to Gray Code Converter .....	5-32
5.8.4	Comparison of Multiplexer and Demultiplexer .....	5-16	5.15.2	BCD to Excess 3 Code Converter .....	5-33
5.8.5	Use of DEMUX in Combinational Logic Design .....	5-16	5.16	Digital (Magnitude) Comparator .....	5-34
5.9	Adders .....	5-18	5.16.1	1-Bit Magnitude Comparator .....	5-35
5.9.1	Half Adder .....	5-18	5.16.2	A 2-bit Comparator .....	5-36
5.9.2	Full Adder .....	5-19	5.17	A 4-Bit Magnitude Comparator (IC 7485) .....	5-37
5.9.3	Full Adder using Half Adders .....	5-20	5.18	Arithmetic Logic Unit (ALU) .....	5-38
5.9.4	Applications of Full Adder .....	5-21	5.19	Decoder .....	5-40
5.10	Binary Subtractors .....	5-21	5.19.1	2 to 4 Line Decoder .....	5-40
5.10.1	Half Subtractor .....	5-21	5.19.2	Difference Between Decoder and Demultiplexer .....	5-41
5.10.2	Full Subtractor .....	5-22	5.19.3	Demultiplexer as Decoder .....	5-41



5.19.4	3 to 8 Line Decoder .....	5-41	5.26	University Questions and Answers .....	5-58
5.19.5	1:8 DEMUX Operated as 3:8 Decoder .....	5-42	5.27	University Questions and Answers (New Syllabus) .....	5-58
5.19.6	IC 74138 (3:8 Decoder) .....	5-42		• <b>Review Questions</b> .....	<b>5-56</b>
5.20	Combinational Logic Design Using Decoders .....	5-43		• <b>MCQs with Answers</b> .....	<b>5-56</b>
5.20.1	BCD to Decimal Decoder .....	5-45	<hr/>		
5.20.2	Advantage of Decoder Realization .....	5-45	<b>Chapter 6 : Flip Flops</b> <span style="float: right;"><b>6-1 to 6-34</b></span>		
5.20.3	Comparison of Realization using Gates, MUX and Decoder .....	5-46	<b>Syllabus</b> : Sequential circuits and systems: A one bit memory, The circuit properties of bistable latch, The clocked SR flip-flop, JK, T, D type Flip-flops, Applications of flip-flops.		
5.21	Standard Logic Functions with MSI Circuits .....	5-47	6.1	Introduction .....	6-2
5.22	Encoders .....	5-47		6.1.1	Clock Signal .....
	5.22.1	Types of Encoders .....		6.1.2	Comparison of Combinational and Sequential Circuits .....
5.23	Priority Encoder .....	5-47		6.2	Latches and Flip-flops .....
	5.23.1	Priority Encoders in the IC Form .....		6.2.1	A 1-Bit Memory Cell (Basic Bistable Element) .....
	5.23.2	Decimal to BCD Encoder .....		6.2.2	The Bistable Multivibrator .....
	5.23.3	Octal to Binary Encoder .....		6.2.3	Latch .....
5.24	Seven Segment LED Display .....	5-50	6.3	Flip Flops / Latches with Active High or Active Low Inputs .....	6-4
	5.24.1	Types of Seven Segment Displays .....		6.3.1	FF / Latches with Active High Inputs .....
	5.24.2	Common Anode Display .....		6.3.2	Flip Flop / Latches with Active Low Inputs .....
	5.24.3	Common Cathode Display .....		6.3.3	S-R Latch using NOR Gates .....
	5.24.4	Use of a Decoder for Driving the Seven Segment Display .....		6.3.4	NAND Latch [S-R Latch using NAND Gates] .....
	5.24.5	Driving a Common Cathode Seven Segment Display .....		6.4	Triggering Methods .....
	5.24.6	BCD to Seven Segment Decoder (Common Anode Display) .....		6.4.1	Concept of Level Triggering .....
5.25	Parity Generators / Checkers .....	5-53		6.4.2	Types of Level Triggered Flip-flops .....
	5.25.1	Parity Generator .....		6.4.3	Concept of Edge Triggering .....
	5.25.2	Parity Checker .....		6.4.4	Comparison of level triggering and edge triggering of flip-flops.....
	5.25.3	Use of EX-OR Gate as a Parity Checker .....		6.4.5	Types of Edge Triggered Flip Flops .....
	5.25.4	A Four Bit Parity Checker using EX-OR Gates .....			





6.5	Gated Latches (Level Triggered SR Flip Flop) .....	6-9	6.12	Toggle Flip Flop (T Flip Flop) .....	6-20
6.5.1	Types of Level Triggered (Clocked) Flip Flops .....	6-10	6.12.1	Positive Edge Triggered T-FF .....	6-20
6.6	The Gated S-R Latch (Clocked S-R Flip Flop) .....	6-10	6.12.2	Negative Edge Triggered T Flip Flop .....	6-21
6.6.1	Negative Level Triggered SR Flip Flop ....	6-11	6.12.3	Application of T F/F .....	6-22
6.6.2	Disadvantage of S-R latch .....	6-11	6.13	Master Slave (MS) JK Flip Flop .....	6-22
6.6.3	Application of S-R latch .....	6-11	6.13.1	Master Slave FF Timing Chart .....	6-23
6.7	Gated D Latch (Clocked D Flip Flop) .....	6-11	6.14	Preset and Clear Inputs .....	6-23
6.8	Gated JK Latch (Level Triggered JK Flip Flop) .....	6-12	6.14.1	S-R Flip-Flop with Preset and Clear Inputs .....	6-24
6.8.1	Race Around Condition in JK Latch .....	6-13	6.14.2	JK Flip Flop with Preset and Clear Inputs .....	6-24
6.8.2	Difference between Latch and Flip-flop .....	6-13	6.14.3	Applications of JK Flip Flop .....	6-25
6.8.3	Pulse Narrowing Circuits for Edge Triggered Flip Flops .....	6-14	6.15	Applications of Flip Flops .....	6-25
6.8.4	A Differentiator Circuit .....	6-14	6.15.1	Application of SR Latch for Elimination of Keyboard Debounce .....	6-25
6.8.5	Pulse Narrowing Circuit for IC Flip Flops .....	6-14	6.16	Excitation Table of Flip-Flop .....	6-26
6.9	Edge Triggered SR Flip-Flops .....	6-15	6.16.1	Excitation Table of SR Flip Flops .....	6-26
6.9.1	Positive Edge Triggered S-R Flip Flop ....	6-15	6.16.2	Excitation Table of D Flip Flop .....	6-27
6.9.2	Negative Edge Triggered S-R Flip Flop .....	6-16	6.16.3	Excitation Table of JK Flip Flop .....	6-27
6.10	Edge Triggered D Flip Flop .....	6-16	6.16.4	Excitation Table of T Flip Flop .....	6-27
6.10.1	Positive Edge Triggered D Flip Flop .....	6-16	6.17	Analysis of Clocked Sequential Circuits .....	6-27
6.10.2	Negative Edge Triggered D Flip Flop .....	6-17	6.17.1	State Table .....	6-28
6.10.3	Applications of D Flip flop .....	6-17	6.17.2	State Diagram .....	6-28
6.11	Edge Triggered J-K Flip Flop .....	6-17	6.17.3	State Equation .....	6-28
6.11.1	Positive Edge Triggered JK Flip Flop .....	6-17	6.18	Design Procedure for Clocked Sequential Circuits .....	6-30
6.11.2	Characteristic Equation of JK Flip Flop .....	6-19	6.19	University Questions and Answers .....	6-34
6.11.3	How does an Edge Triggered JK FF Avoid Race Around Condition ? .....	6-19	6.20	University Questions and Answers (New Syllabus) .....	6-34
6.11.4	Negative Edge Triggered JK Flip-Flop .....	6-19		• <b>Review Questions</b> .....	<b>6-31</b>
				• <b>MCQs with Answers</b> .....	<b>6-32</b>

**Chapter 7 : Shift Registers 7-1 to 7-20**

**Syllabus :** Shift registers, Applications of shift registers  
Serial to parallel converter, Parallel to serial converter, Ring  
counter, Sequence generator.

7.1	Introduction .....	7-2
7.2	Data Formats .....	7-2
7.3	Classification of Registers .....	7-2
7.4	Buffer Registers .....	7-2
7.5	Shift Registers .....	7-3
7.5.1	Serial Input Serial Output (Shift Left Mode) .....	7-4
7.5.2	Serial In Serial Out (Shift Right Mode) .....	7-5
7.5.3	Applications of Serial Operation .....	7-7
7.6	Serial In Parallel Out (SIPO) .....	7-7
7.7	Parallel In Serial Out Mode (PISO) .....	7-7
7.8	Parallel In Parallel Out (PIPO) .....	7-8
7.9	Bidirectional Shift Register .....	7-8
7.9.1	A 3-bit Bidirectional Register using the JK Flip Flops .....	7-9
7.10	Universal Shift Register .....	7-9
7.10.1	Universal Shift Register using Multiplexers and D-flip flops .....	7-10
7.11	MSI Shift Registers and their Applications .....	7-11
7.11.1	Universal Shift Register IC 7495 .....	7-11
7.11.2	Parallel Loading (PIPO) .....	7-13
7.11.3	Serial Shift Right Operation .....	7-13
7.11.4	Serial Shift Left Operation .....	7-13
7.12	Applications of Shift Registers .....	7-14
7.12.1	Serial to Parallel Converter .....	7-14
7.12.2	Parallel to Serial Converter .....	7-14
7.12.3	Ring Counter .....	7-14

7.12.4	Johnson's Counter (Twisted / Switch Tail Ring Counter) .....	7-15
7.12.5	Johnson's Counter using D Flip-flops .....	7-17
7.12.6	Sequence Generator .....	7-17
7.13	Solved Examples .....	7-17
7.14	University Questions and Answers (New Syllabus) .....	7-20
	• <b>Review Questions</b> .....	<b>7-19</b>
	• <b>MCQs with Answers</b> .....	<b>7-19</b>

**Chapter 8 : Counters 8-1 to 8-40**

**Syllabus :** Ripple (Asynchronous) counters, Synchronous  
counters, Counters design using flip-flops, Special counter  
IC's, Asynchronous sequential counters, Applications of  
counters.

8.1	Introduction .....	8-2
8.1.1	Types of Counters .....	8-2
8.1.2	Classification of Counters .....	8-2
8.2	Asynchronous/Ripple Up Counters .....	8-2
8.2.1	3 Bit Asynchronous Up Counter .....	8-4
8.2.2	4 Bit Asynchronous up Counter .....	8-5
8.2.3	State Diagram of a Counter .....	8-6
8.3	Asynchronous Down Counters .....	8-6
8.3.1	3- Bit Asynchronous Down Counter .....	8-6
8.4	UP / DOWN Counters .....	8-8
8.4.1	UP/DOWN Ripple Counters .....	8-8
8.4.2	3-bit and 4-bit Up Down Ripple Counters .....	8-8
8.5	Modulus of the Counter (MOD-N Counter) .....	8-10
8.5.1	Frequency Division Taking Place in Asynchronous Counters .....	8-13
8.5.2	Decade (BCD) Ripple Counter .....	8-13
8.5.3	Disadvantages of Ripple Counters .....	8-14
8.6	Specialized Counter ICs .....	8-15

8.6.1	Ripple Counter IC 7490 (Decade Counter) .....	8-15
8.6.2	IC 7493 (4- bit Binary Counters) .....	8-18
8.7	Synchronous Counters .....	8-21
8.7.1	2-Bit Synchronous up Counter .....	8-21
8.7.2	3-Bit Synchronous Binary up Counter .....	8-22
8.7.3	Design of the 3 Bit Synchronous Counter .....	8-23
8.7.4	Four Bit Synchronous Up Counter .....	8-25
8.8	Modulo – N Synchronous Counters .....	8-26
8.8.1	Synchronous Decade Counter .....	8-26
8.9	UP / DOWN Synchronous Counter .....	8-30
8.9.1	3-bit Up/Down Synchronous Counter .....	8-30
8.10	Sequential Counters .....	8-31
8.10.1	Design of a Counter using State Diagram .....	8-31
8.10.2	Lock Out Condition in a Counter .....	8-31
8.10.3	Bush Diagram for Sequence Counter .....	8-34
8.10.4	Advantages of Synchronous Counter .....	8-34
8.10.5	Comparison of Synchronous and Asynchronous Counters .....	8-35
8.10.6	Comparison of Counter and Shift Register .....	8-35
8.11	Special Synchronous Counter ICs .....	8-35
8.11.1	IC 74193 (UP/DOWN Modulo-16 Binary Counter) .....	8-35
8.12	Applications of Counters .....	8-38
8.13	University Questions and Answers .....	8-40
8.14	University Questions and Answers (New Syllabus) .....	8-40
	• <b>Review Questions</b> .....	<b>8-38</b>
	• <b>MCQs with Answers</b> .....	<b>8-38</b>

**Chapter 9 : D/A and A/D Converters 9-1 to 9-32**

**Syllabus** : Digital to analog converters : Weighed resistor/converter, R/2R ladder D/A converter, specifications of D/A converters, Examples of D/A converter ICs, Sample and hold circuit, Analog to digital converters : Quantization and encoding, Parallel comparator A/D converter, Successive approximation A/D converter, Counting A/D converter, Dual slope A/D converter, A/D converter using voltage to frequency and voltage to time conversion, Specifications of A/D converters, Examples of A/D converters ICs.

9.1	Introduction .....	9-2
9.2	Types of Data Converters .....	9-2
9.3	Variable Resistor Networks .....	9-2
9.3.1	Binary Equivalent Weight (B.E.W.) .....	9-2
9.4	Resistive Dividers .....	9-3
9.4.1	Binary Weighted Resistor Network .....	9-4
9.4.2	Full Scale Output $V_{FS}$ .....	9-4
9.5	D/A Converters .....	9-4
9.5.1	Types of D to A Converters .....	9-5
9.6	Binary Weighted Resistor DAC .....	9-5
9.7	Binary Ladder (R-2R Ladder Network) .....	9-7
9.7.1	R-2R Ladder DAC .....	9-8
9.7.2	Comparison of DACs .....	9-10
9.8	Specifications of DAC .....	9-11
9.8.1	Resolution .....	9-11
9.8.2	Accuracy .....	9-11
9.8.3	Linearity .....	9-11
9.8.4	Temperature Sensitivity .....	9-12
9.8.5	Settling Time .....	9-12
9.8.6	Speed .....	9-12
9.8.7	Long Term Drift .....	9-12
9.8.8	Supply Rejection .....	9-12

